MADHAVAN S

Electronics & Communication Engineer
DSP – RTL Design & Verification

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SUMMARY

Electronics & Communication Engineering undergraduate at PSG iTech, also pursuing a B.S. in Electronic Systems at IIT Madras, with experience in digital communication algorithms, signal processing, MATLAB Simulink, and digital hardware development. Hands - on in QPSK, QAM, OFDM and BER analysis, with additional experience in MFCC and spectral feature extraction for an IEEE published voice detection system. Hardware Research Intern at DRDO with experience in ADC based signal acquisition and real-time protection systems. Interested in wireless algorithm development, DSP and digital IP design for next generation communication systems.

EDUCATION

PSG Institute of Technology and Applied Research 2023 – 2027 (expected)
B.E. Electronics and Communication Engineering - CGPA: 8.22 (until 6th semester)

Indian Institute of Technology, Madras 2023 – 2027 (expected)
B.S. Electronics Systems (Hybrid) - CGPA: 8.00 (until now)

ARB International School 2022 – 2023
Higher Secondary (Grade 12) - Percentage: 95.2%

AREAS OF INTEREST

○ RTL Design & Verification ○ Digital IC Design ○ DSP ○ Signal Processing ○ Agentic AI

SKILLS

HDL & Programming: Verilog, C, Embedded C, Assembly, Python (basic)
EDA & Tools: Xilinx Vivado, Cadence Virtuoso, STM32CubeIDE, MATLAB, MATLAB Simulink
Hardware: STM32F407, Zedboard Zynq 7000 (FPGA), Raspberry Pi, ESP32
Soft Skills: Leadership, Organising, Communication, Problem Solving

EXPERIENCE

Hardware Research Intern May 2026 – July 2026
Defence Research and Development Organization (CVRDE), Govt. of India, Avadi (On-site)
- Designed solid-state power controller hardware interface using an STM32F407, isolated gate driver, power MOSFET and Kelvin-shunt current sensing; interfaced the conditioned signal with 12-bit ADC for real-time current telemetry.
- Implemented dual-path overcurrent protection combining firmware-based I^2t monitoring with hardware desaturation (DESAT) protection; validated the ADC interface using STM32CubeIDE.

AI/IoT Intern July 2025 – Jan 2026
Do365 Technologies, RS Puram, Coimbatore (Hybrid)
- Developed and deployed an AI-based attendance system on Raspberry Pi 5, integrating custom YOLOv8 person detection, MobileNetV2 verification, and anti-spoofing to detect photo/screen-based impersonation; achieved 96% detection accuracy.
- Developed an IoT-based automated attendance workflow for real-time attendance logging across company campus and mess facilities.

PUBLICATIONS

Real-Time Detection of AI-Generated Voice Using Machine Learning and MATLAB Simulink
DOI: 10.1109/ICIIET65921.2025.11379238 *IEEE ICIIET 2025*
- Developed a real-time AI-generated voice detection pipeline in MATLAB Simulink, extracting 26 audio features using MFCC and spectral features from 25 ms windows with 10 ms hop.
- Trained a 60-tree Random Forest achieving 92.3% accuracy, 93.8% recall, and 180 ms CPU inference latency, outperforming CNN/LSTM models under deployment constraints.

A Deep Learning Framework for Spatiotemporal Air Quality Forecasting Using Episode Aware Optimization
DOI: 10.1109/ICSSEECC69062.2026.11721986 *IEEE IC(SEC)^2 2026*
- Developed a lightweight ConvLSTM2D encoder-decoder for 16-hour PM2.5 forecasting using WRF-Chem data, incorporating episode-aware weighting and residual skip connections.
- Achieved 0.946 Pearson correlation, 18.24 $\mu g/m^3$ RMSE, and 88% AQI classification accuracy with only 402K trainable parameters.

ACHIEVEMENT

First Runner-up – SAP LABS Hackfest'26 Prize: Rs. 75,000
Built an agentic AI system for VLSI design verification capable of autonomous verification and correction through to the fabrication-ready stage.

DVCon India '26 Fellowship 2026
Selected as a DVCon India Fellow for the Design and Verification Conference (DVCon) 2026, recognising research interest towards RTL verification and hardware design.

Young Innovator Award – PSG iTech '26 2026
Received the award at the annual Daksha 2026 summit for leading innovative projects, securing top positions in hackathons and achieving strong academic performance.

PROJECTS

Power Grid Monitoring & Protection System *Embedded Systems, Signal Processing, ML*
- Designed a 230 V AC monitoring system using a bridge rectifier, low-pass filter and voltage divider for ESP32 ADC interfacing and frequency measurement.
- Developed DNN-based fault classification on Raspberry Pi using temporal signal parameters, with relay-based automatic load disconnection and restoration.

Gated Dual-Coordinate Relative Position Attention (GD-CoRPA) *Semiconductor, Computer Vision*
- Developed lightweight CNN–Vision Transformer hybrid for nine-class semiconductor wafer defect classification, incorporating a custom attention mechanism that blends Cartesian and polar spatial relationships using a learned gate.
- Achieved 98.86% test accuracy and 0.9886 macro-F1 on 5,607 wafer images using a 2.49M-parameter model.

RTL Verification Impact and Coverage-Gap Framework (VIGIL-AI) *VLSI, RTL Verification, Agentic AI*
- Developed an AI-assisted RTL verification framework that compares RTL revisions, identifies modified modules, and analyses downstream impact to prioritise regression testing.
- Identifies potential coverage gaps and corner cases involving boundary conditions, FSM transitions and interface behaviour, generating actionable verification reports.

Adaptive SoC Verification Framework (ASVF) *EDA, RTL Verification, Agentic AI*
- Proposed an AI-assisted verification framework combining SystemVerilog Assertion (SVA) proof classification, clock-domain crossing (CDC) risk analysis, and waveform-based failure diagnosis.
- Designed an architecture integrating GraphSAGE, Random Forest and transformer-based models through an agent pipeline for verification prioritisation and root-cause analysis.

IoT-enabled Soil Monitoring & Crop Recommendation System *IoT, Embedded Systems, ML*
- Developed an ESP32-based soil-monitoring system integrating NPK, pH and soil-moisture sensors with real-time and historical data processing.
- Built an ML pipeline for soil classification and crop recommendation, achieving 94% accuracy and presenting results through a web interface.

LEADERSHIP & OUTREACH

Hackathon Organizer – iTECH Summit, YUKTA 2K26 2026
PSG Institute of Technology and Applied Research
Organised a 3 round inter college hackathon with 500+ Round 1 participants, managing judging coordination and participant communication; received the Organizing Excellence Award 2026 from the Principal.

Student Mentor February 2026
DMI Engineering College, Nagercoil
Invited as a guest speaker for the Student Mentorship Programme; delivered a career guidance session on hackathons, competitions, academics, and career development.

Industrial Visit Coordinator 2024 & 2025
PSG Institute of Technology and Applied Research
Organised and managed industrial visits for 100+ students across two consecutive years, coordinating travel, accommodation, itineraries and end to end logistics.